Fifty Nifty Variations of Two-Transistor Circuits

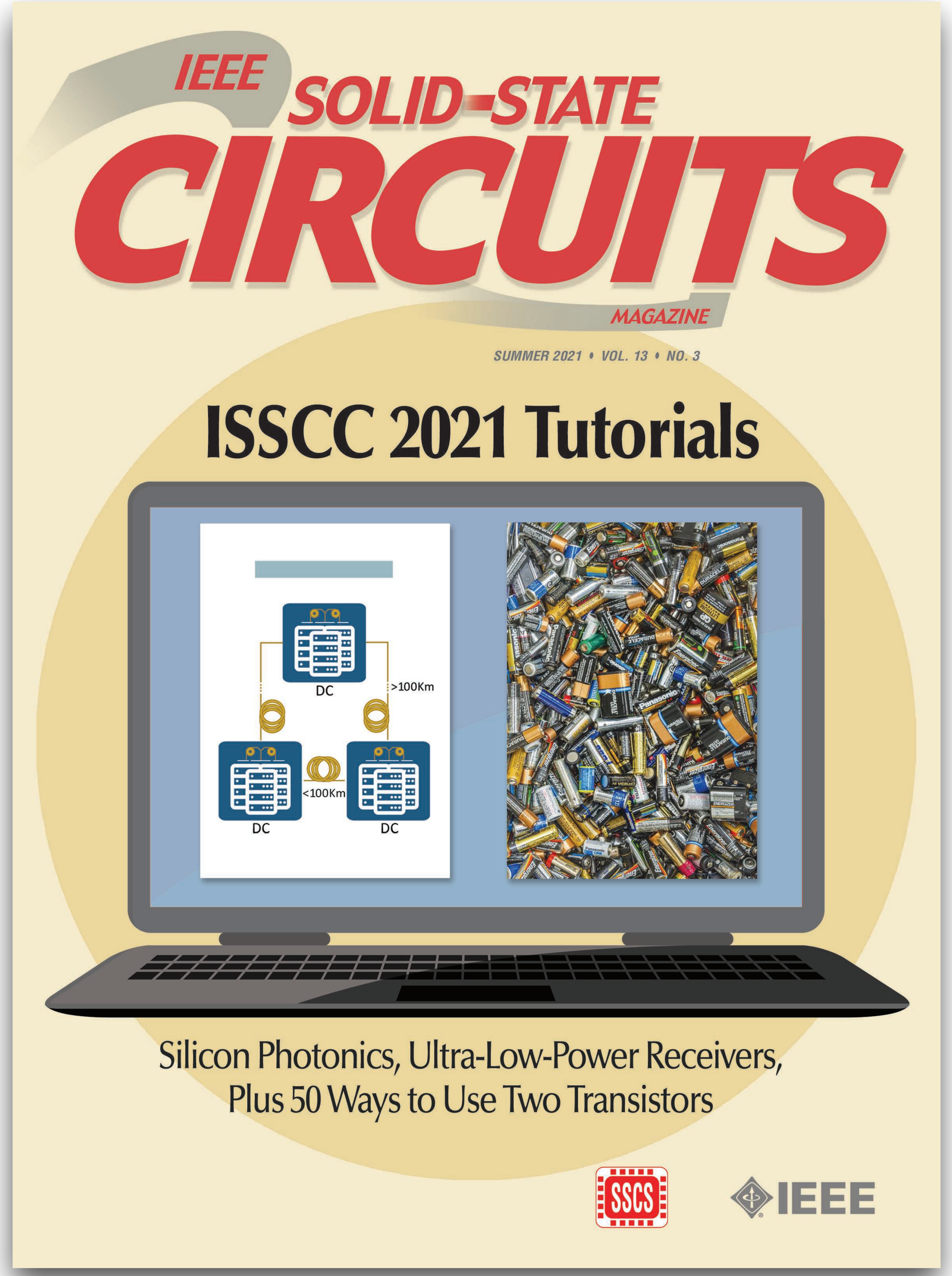
Harald Pretl (harald.pretl@jku.at)

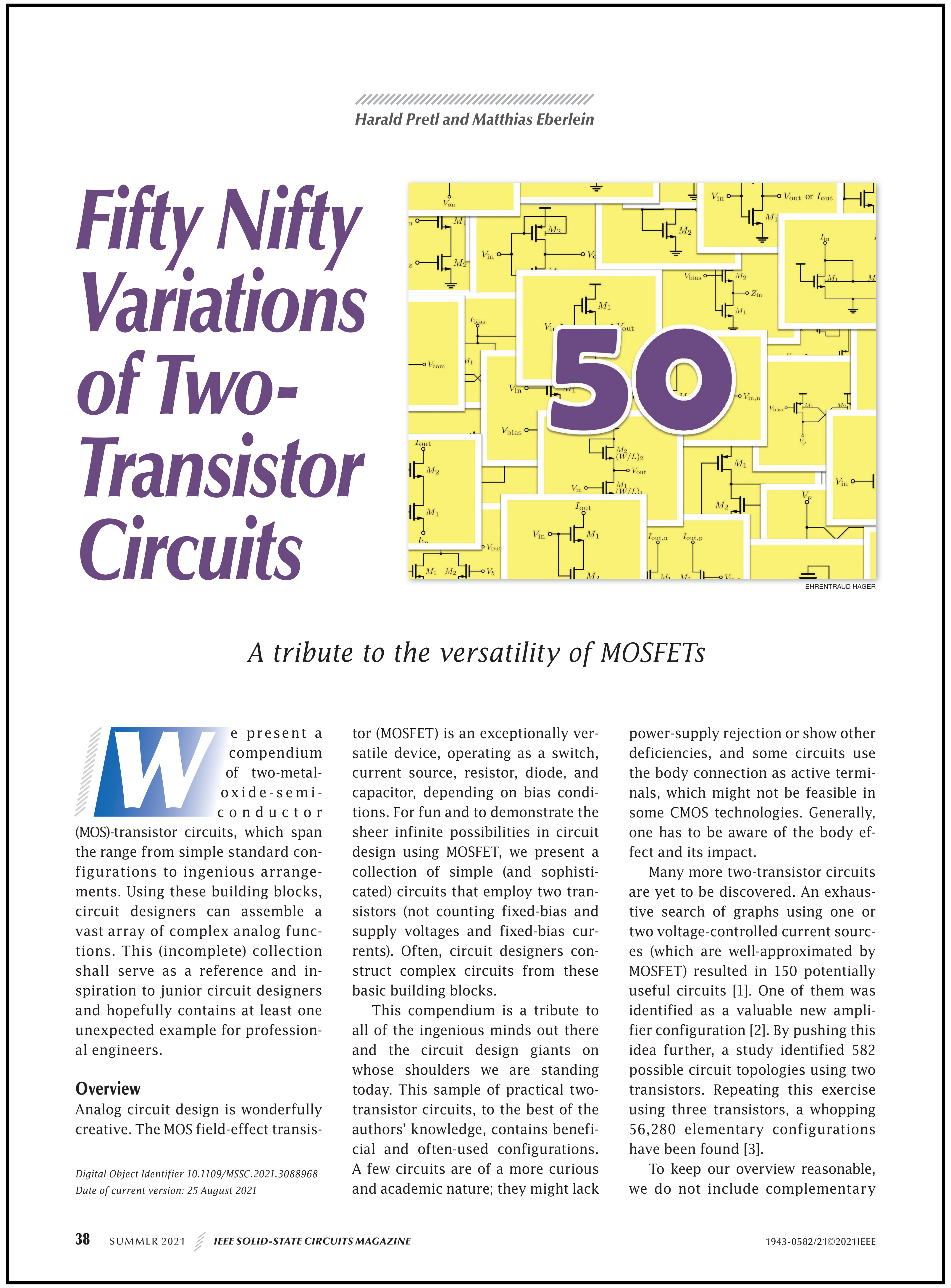
JOHANNES KEPLER UNIVERSITY LINZ

MOS-AK Workshop Spring 2022

INSTITUTE FOR INTEGRATED CIRCUITS

Why am I Here? You Might Have Seen This…





Harald Pretl and Matthias Eberlein

Fifty Nifty Variations of Two-Transistor Circuits

EHRENTRAUD HAGER

A tribute to the versatility of MOSFETs

We present a compendium of two-metal-oxide-semiconductor (MOS)-transistor circuits, which span the range from simple standard configurations to ingenious arrangements. Using these building blocks, circuit designers can assemble a vast array of complex analog functions. This (incomplete) collection shall serve as a reference and inspiration to junior circuit designers and hopefully contains at least one unexpected example for professional engineers.

Overview

Analog circuit design is wonderfully creative. The MOS field-effect transistor (MOSFET) is an exceptionally versatile device, operating as a switch, current source, resistor, diode, and capacitor, depending on bias conditions. For fun and to demonstrate the sheer infinite possibilities in circuit design using MOSFET, we present a collection of simple (and sophisticated) circuits that employ two transistors (not counting fixed-bias and supply voltages and fixed-bias currents). Often, circuit designers construct complex circuits from these basic building blocks.

This compendium is a tribute to all of the ingenious minds out there and the circuit design giants on whose shoulders we are standing today. This sample of practical two-transistor circuits, to the best of the authors' knowledge, contains beneficial and often-used configurations. A few circuits are of a more curious and academic nature; they might lack power-supply rejection or show other deficiencies, and some circuits use the body connection as active terminals, which might not be feasible in some CMOS technologies. Generally, one has to be aware of the body effect and its impact.

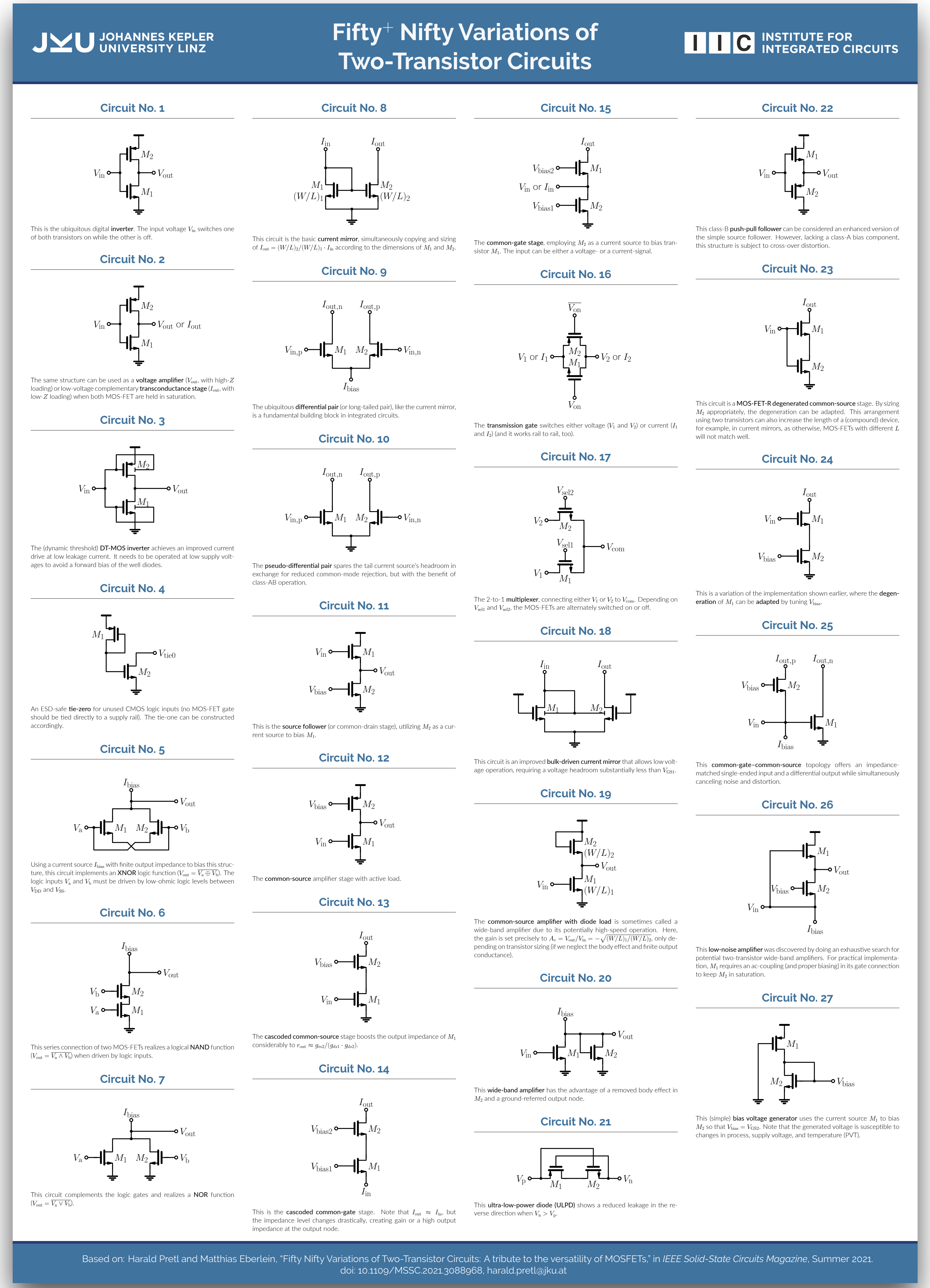
Many more two-transistor circuits are yet to be discovered. An exhaustive search of graphs using one or two voltage-controlled current sources (which are well-approximated by MOSFET) resulted in 150 potentially useful circuits [1]. One of them was identified as a valuable new amplifier configuration [2]. By pushing this idea further, a study identified 582 possible circuit topologies using two transistors. Repeating this exercise using three transistors, a whopping 56,280 elementary configurations have been found [3].

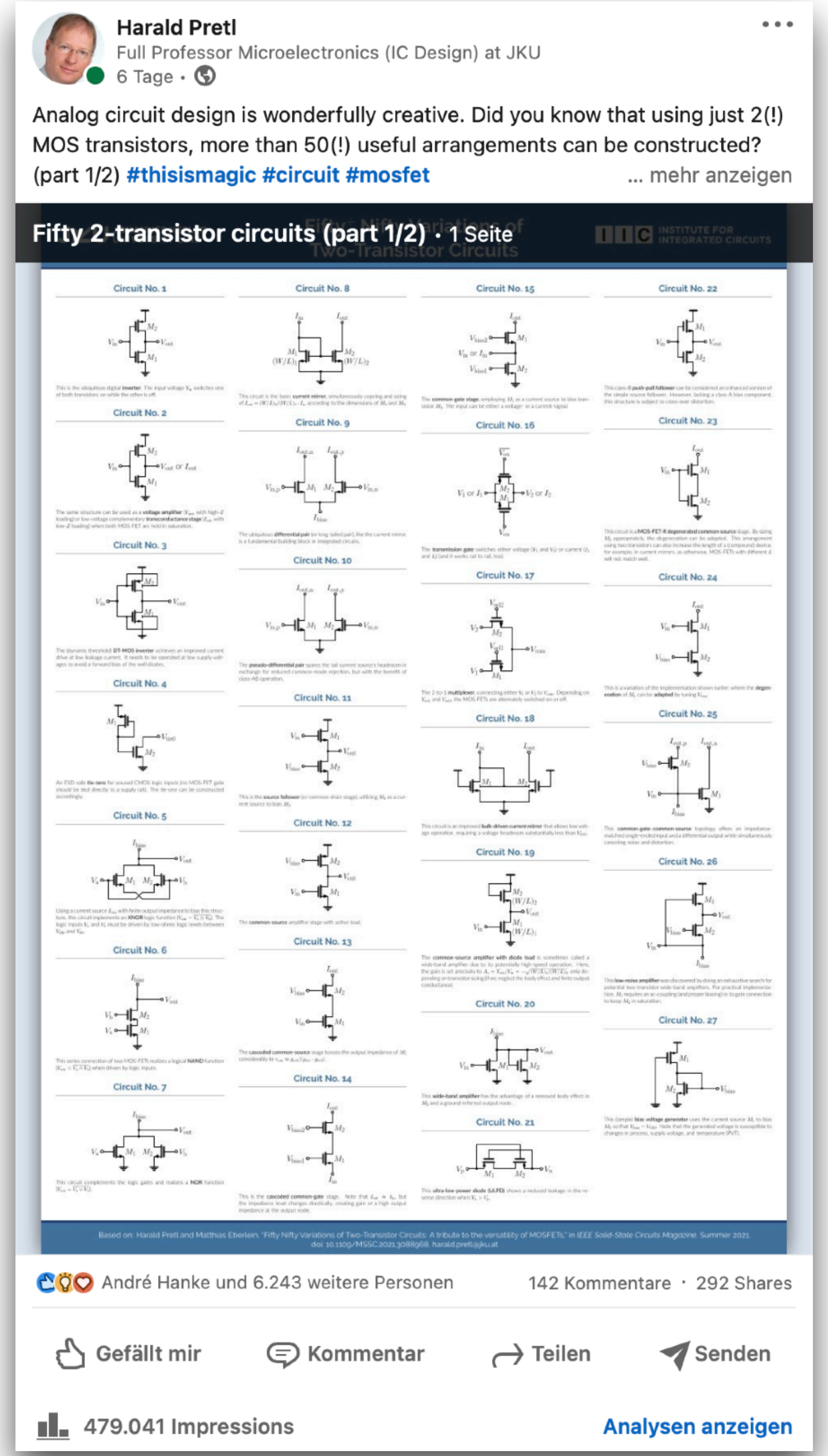
To keep our overview reasonable, we do not include complementary

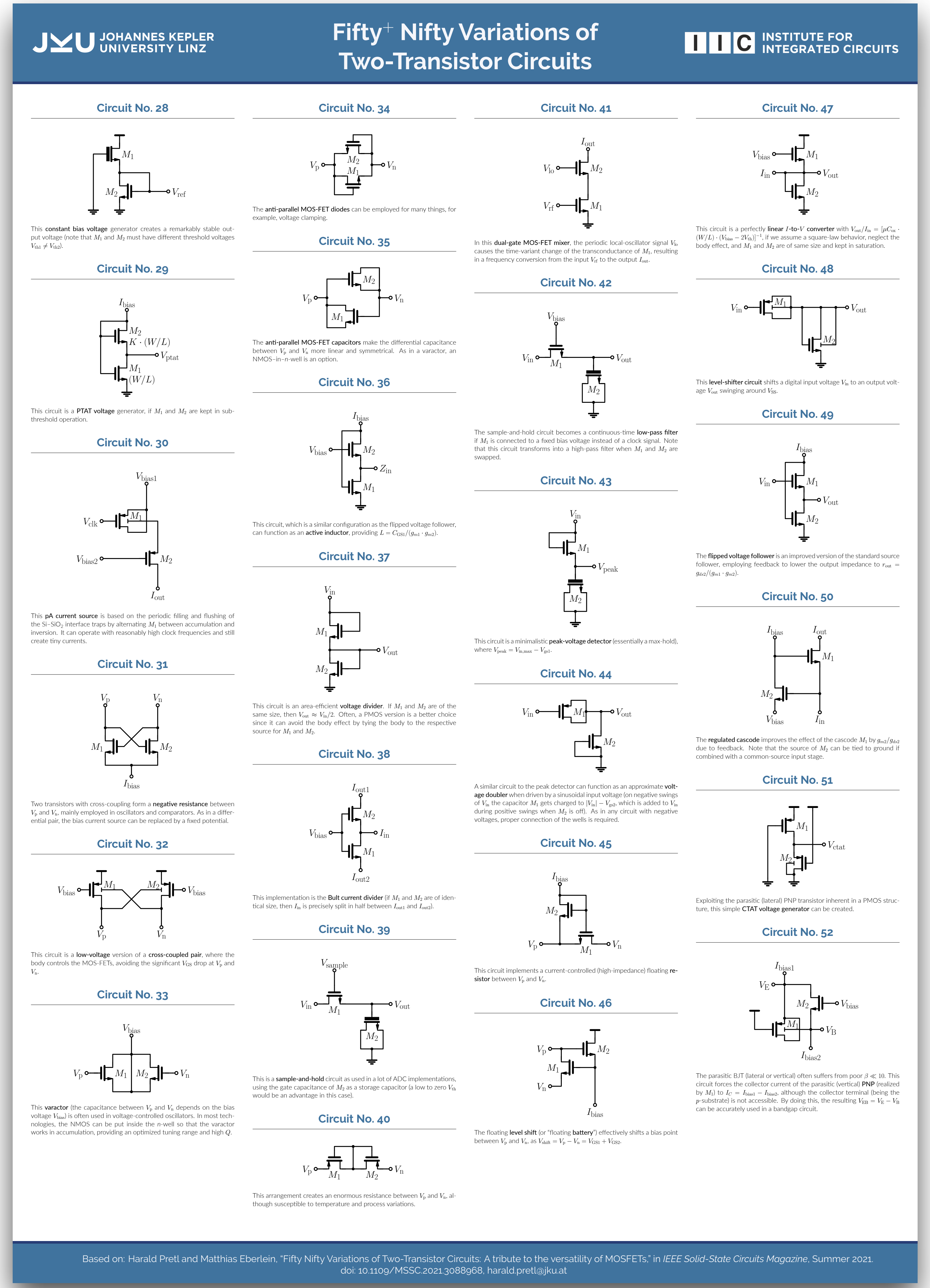
Digital Object Identifier 10.1109/MSSC.2021.3088968
Date of current version: 25 August 2021

[1]

… Or This?

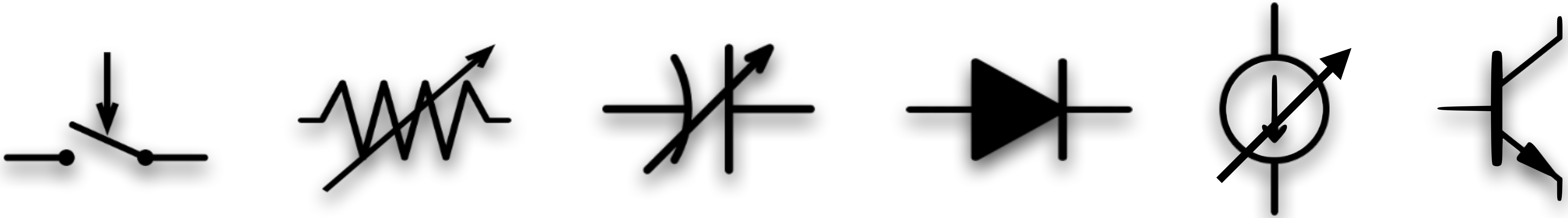

JOHANNES KEPLER UNIVERSITY LINZ
Fifty+ Nifty Variations of Two-Transistor Circuits
INSTITUTE FOR INTEGRATED CIRCUITS
Based on: Harald Pretl and Matthias Eberlein, "Fifty Nifty Variations of Two-Transistor Circuits: A tribute to the versatility of MOSFETs," in IEEE Solid-State Circuits Magazine, Summer 2021.
doi: 10.1109/MSSC.2021.3088968, harald.pretl@jku.at


Harald Pretl
Full Professor Microelectronics (IC Design) at JKU
6 Tage •
Analog circuit design is wonderfully creative. Did you know that using just 2(!) MOS transistors, more than 50(!) useful arrangements can be constructed? (part 1/2) #thisismagic #circuit #mosfet
… mehr anzeigen
Fifty 2-transistor circuits (part 1/2) • 1 Seite
André Hanke und 6.243 weitere Personen
142 Kommentare • 292 Shares
Gefällt mir
Kommentar
Teilen
Senden
479.041 Impressions
Analysen anzeigen


JOHANNES KEPLER UNIVERSITY LINZ
Fifty+ Nifty Variations of Two-Transistor Circuits
INSTITUTE FOR INTEGRATED CIRCUITS
Based on: Harald Pretl and Matthias Eberlein, "Fifty Nifty Variations of Two-Transistor Circuits: A tribute to the versatility of MOSFETs," in IEEE Solid-State Circuits Magazine, Summer 2021.
doi: 10.1109/MSSC.2021.3088968, harald.pretl@jku.at

Why Write Such an Article?

- It is fun, and a celebration of engineers' ingenuity and creativity!
- It shows the versatility of the MOSFET. Depending on bias conditions, it works as



- So a couple of years ago a thought appeared:

  „How many circuits with 2 transistors are there?“ — and we started collecting.

Some Tried to Systematically Find Useful Circuits

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING, VOL. 48, NO. 11, NOVEMBER 2001 1039

Finding All Elementary Circuits Exploiting Transconductance

Eric A. M. Klumperink, *Member, IEEE*, Federico Bruccoleri, *Student Member, IEEE*, and Bram Nauta, *Member, IEEE*

***Abstract*—Commonly used elementary circuits like single-transistor amplifier stages, the differential pair, and current mirrors basically exploit the transconductance property of transistors. This paper aims at finding all elementary transconductance-based circuits. For this purpose, all graphs of two-port circuits with one or two voltage controlled current sources are generated systematically. This results in 150 graphs of "finite transactance two-port circuits" with at least one nonzero transmission parameter. Each of them can be implemented in various ways using transistors and resistors, covering many commonly required types of two-ports. To illustrate the usefulness of the technique several alternative circuit implementations for current amplifiers and voltage followers are generated. A new wide-band low-noise amplifier generated with the technique was realized in 0.35-μm CMOS.**

***Index Terms*—Analog circuit design, circuit synthesis, circuit topology, computer-aided design, systematic circuit generation, transconductor, voltage-controlled current source.**

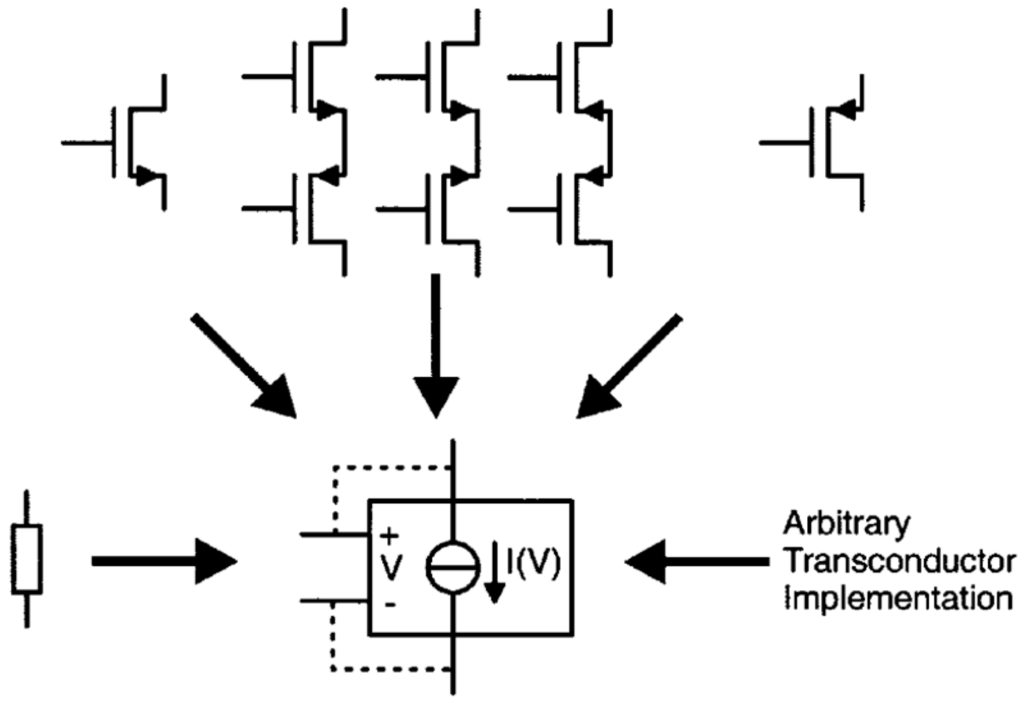


Fig. 1. In many circuits transistor and resistor configurations are exploited as a transconductor and can be modeled by a voltage controlled current source (VCCS).

[2]

118 CANADIAN JOURNAL OF ELECTRICAL AND COMPUTER ENGINEERING, VOL. 41, NO. 3, SUMMER 2018

Method of Generating Unique Elementary Circuit Topologies
Méthode de génération de topologies de circuits élémentaires uniques

Delaram Shahhosseini, Eugene Zailer, *Student Member, IEEE*, Laleh Behjat, *Senior Member, IEEE*, and Leonid Belostotski, *Senior Member, IEEE*

***Abstract*—Designing analog circuits with new topologies is often very challenging, as it requires not only circuit design expertise but also an intuition of how various elementary circuits may work when put together to form a larger circuit. In this paper, we present a method of generating all functional *elementary* circuit topologies. This**

582 two-transistor and 56 280 three-transistor

designers by both offering previously unknown circuit topologies and providing circuit topologies for further optimizations. To give an example of how this vision can be used in practice, a search for all amplifier circuits was conducted that resulted in 5177 circuit topologies, some previously unknown, out of 56 862 three-transistor elementary circuit topologies.

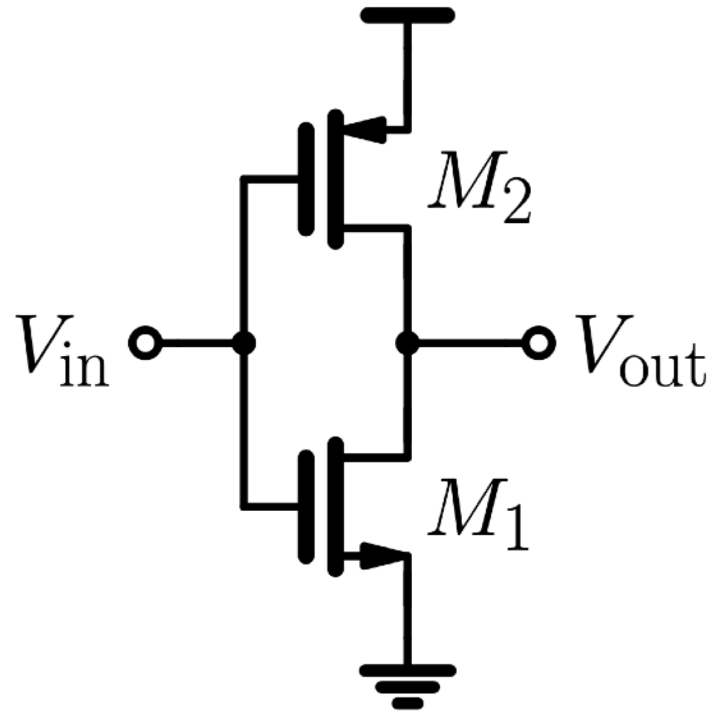
***Résumé*—La conception de circuits analogiques avec de nouvelles topologies est souvent très difficile car elle nécessite non seulement une expertise en conception de circuits, mais aussi une intuition de la façon dont différents circuits élémentaires peuvent fonctionner lorsqu'ils forment un plus grand circuit. Dans cet article, nous présentons une méthode de génération de toutes les topologies de circuits élémentaires fonctionnels. Cet article utilise la combinatoire pour garantir que toutes les topologies de circuits uniques sont générées et stockées dans une base de données. Cette base de données contient 582 topologies de circuits élémentaires fonctionnels et uniques à deux transistors et 56 280 à trois transistors. Il est envisagé que les topologies de circuit stockées dans la base de données permettent d'économiser du temps de conception et d'aider les concepteurs à la fois à offrir des topologies de circuits inconnues et à fournir des topologies de circuits pour d'autres optimisations. Pour donner un exemple de la façon dont cette vision peut être utilisée dans la pratique, une recherche de tous les circuits amplificateurs a été effectuée.**

***Index Terms*—Analog circuit synthesis, computer-aided design, integrated circuit design, mathematical programming.**

[3]

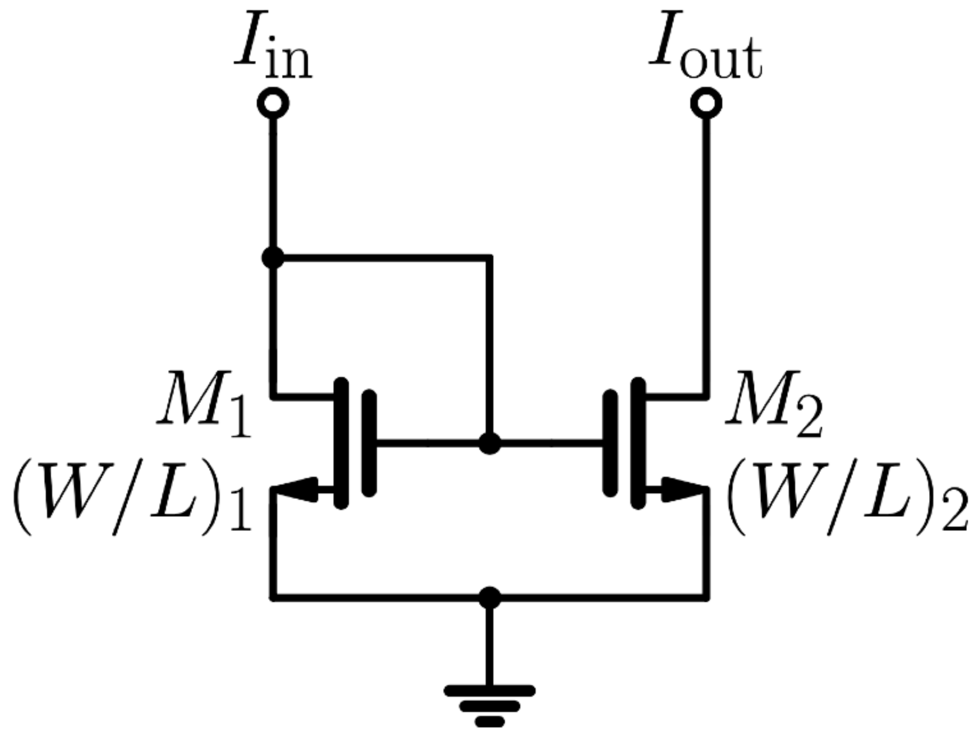
Now Let’s Look Into the 50 Circuit Snippets we Collected

Quite a Few are Well-Known Classics



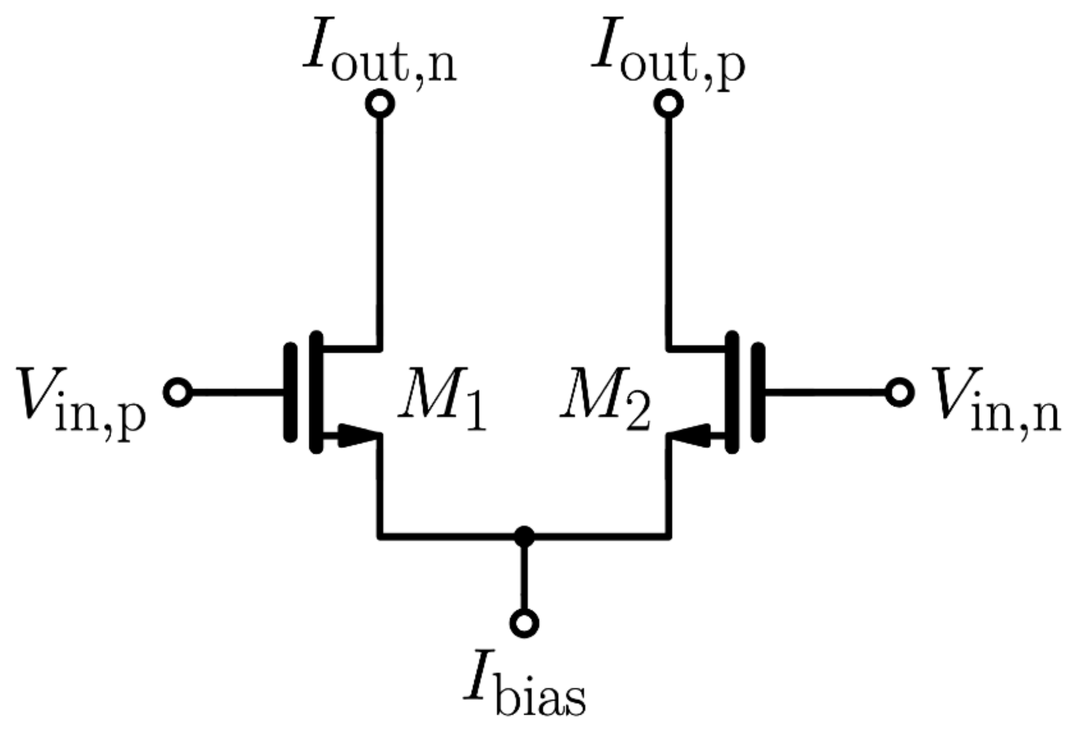
[4]

This is the ubiquitous digital **inverter**. The input voltage V_{in} switches one of both transistors on while the other is off.



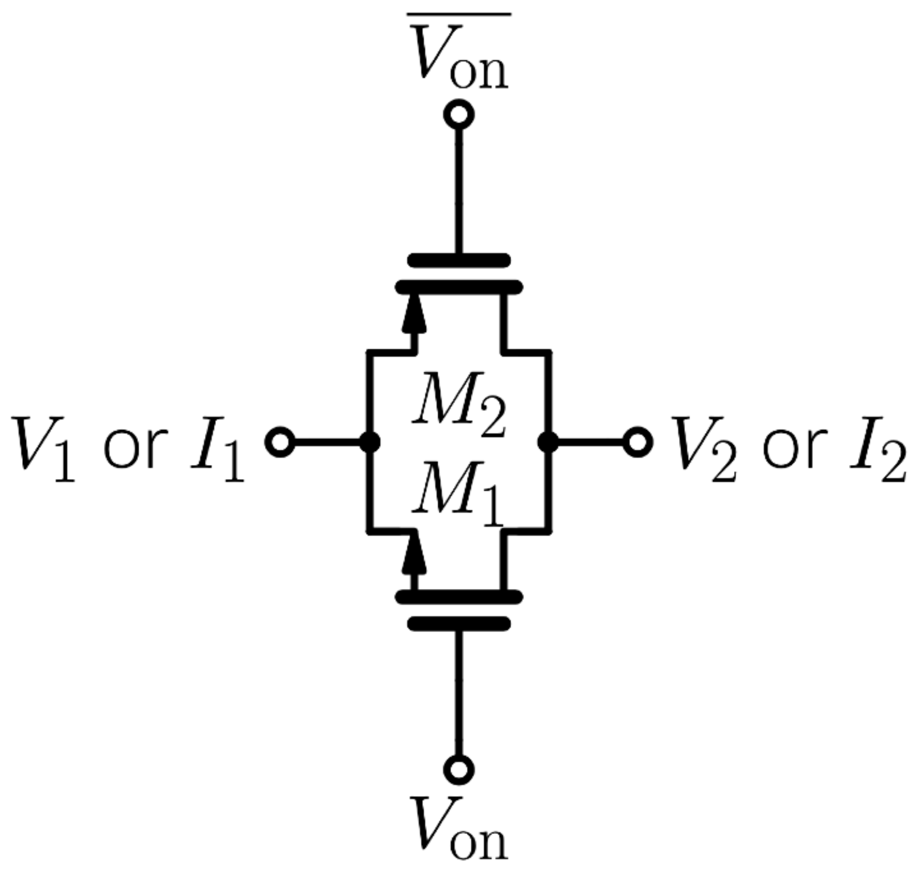
[5]

This circuit is the basic **current mirror**, simultaneously copying and sizing of $I_{\text{out}} = (W/L)_2/(W/L)_1 \cdot I_{\text{in}}$ according to the dimensions of M_1 and M_2.



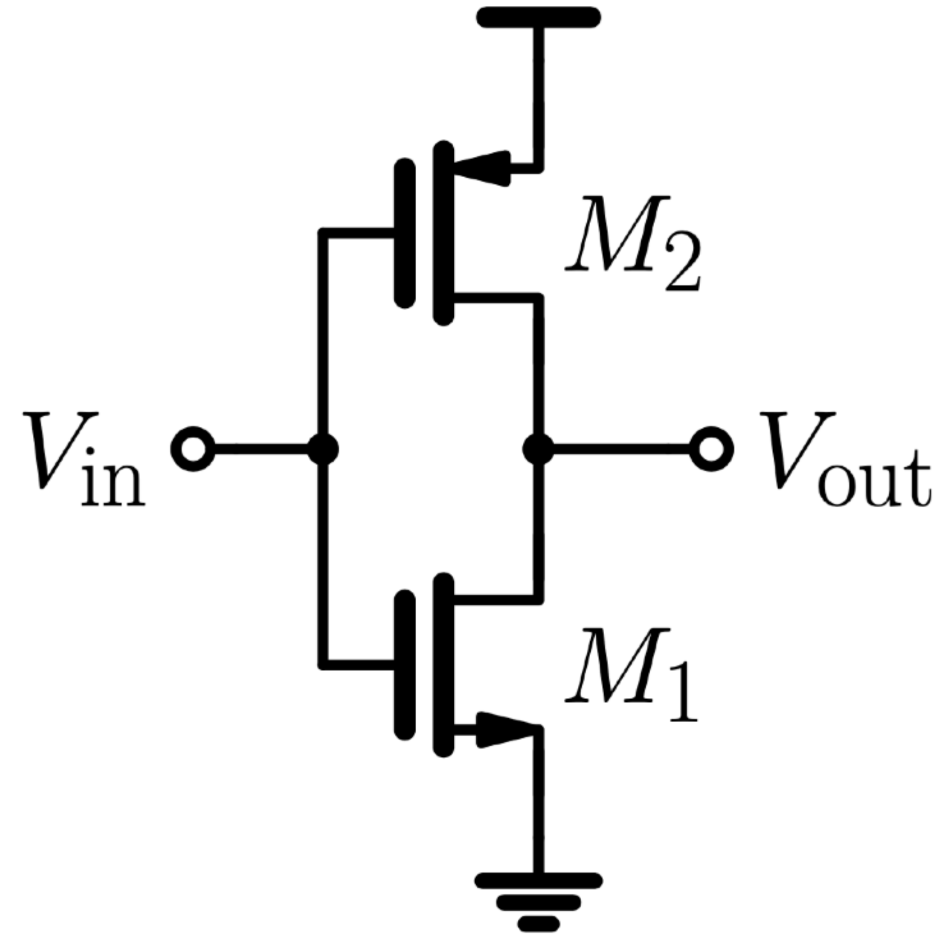
[6]

The ubiquitous **differential pair** (or long-tailed pair), like the current mirror, is a fundamental building block in integrated circuits.

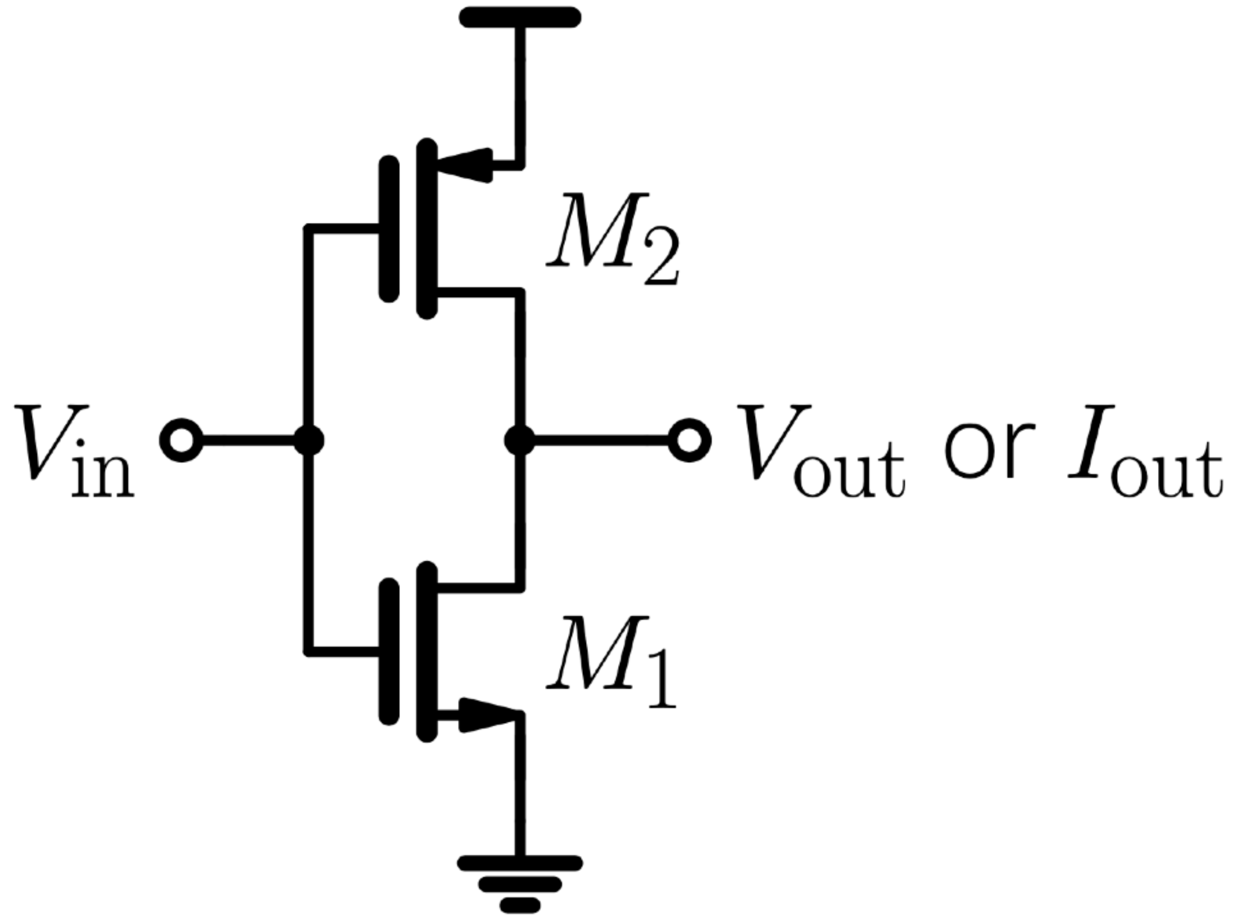


The **transmission gate** switches either voltage (V_1 and V_2) or current (I_1 and I_2) (and it works rail to rail, too).

Some Have a Dual-Use Not-That-Obvious



[4]

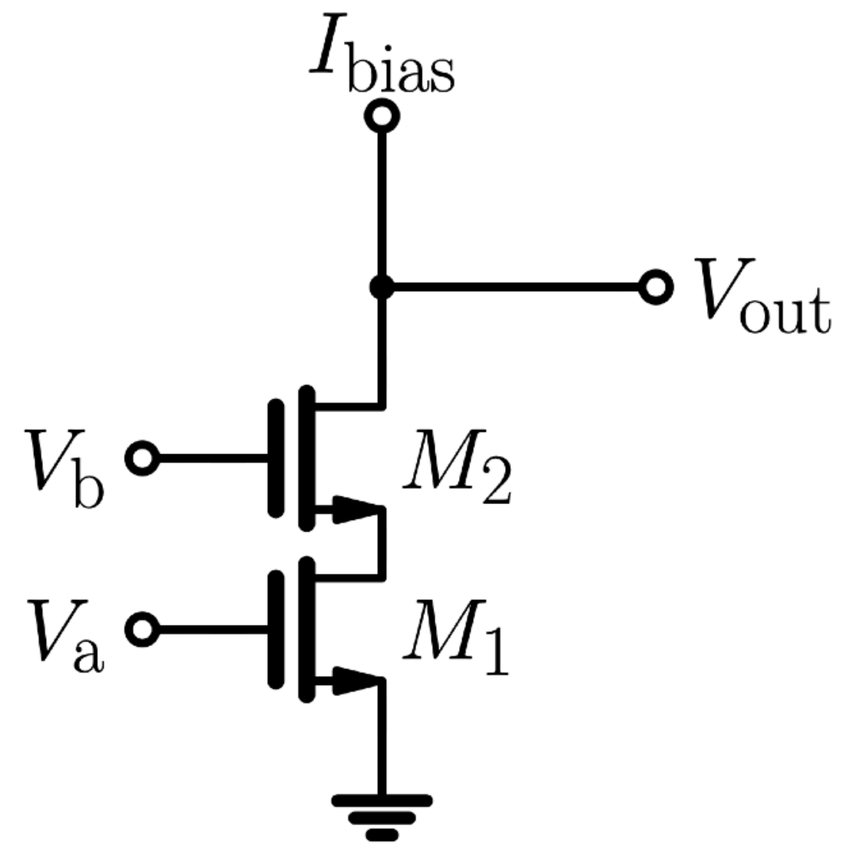


[7,8]

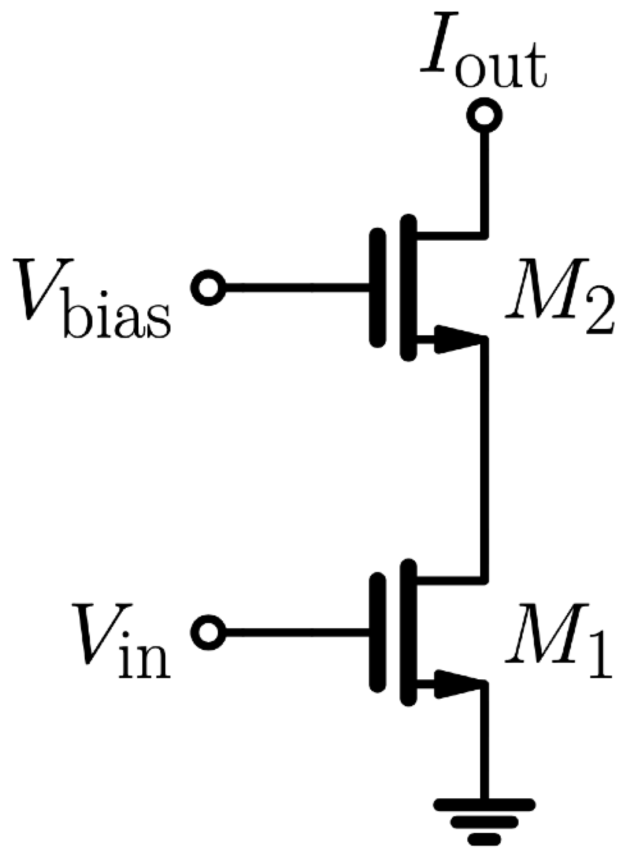
This is the ubiquitous digital **inverter**. The input voltage V_{in} switches one of both transistors on while the other is off.

The same structure can be used as a **voltage amplifier** (V_{out}, with high-Z loading) or low-voltage complementary **transconductance stage** (I_{out}, with low-Z loading) when both MOS-FET are held in saturation.

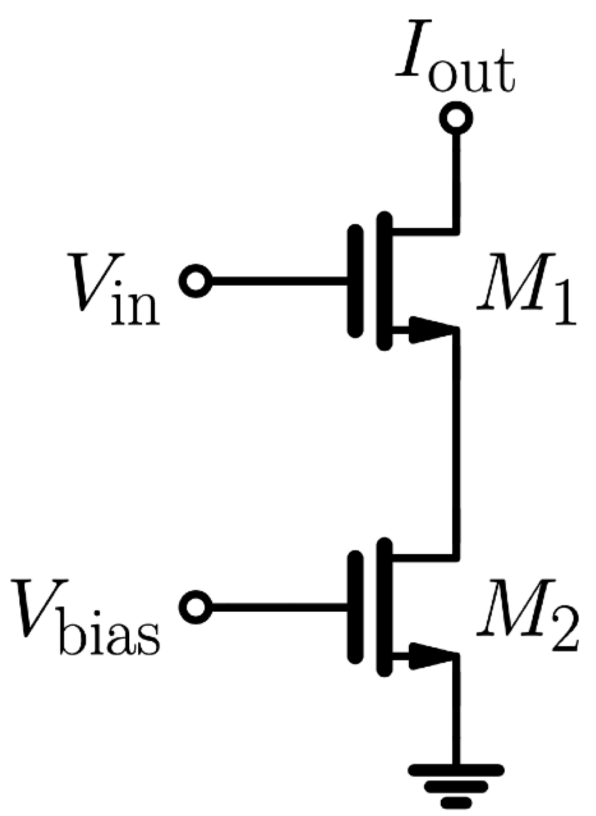
Same Arrangement, Different Application



This series connection of two MOS-FETs realizes a logical **NAND** function ($V_{\text{out}} = \overline{V_{\text{a}} \wedge V_{\text{b}}}$) when driven by logic inputs.

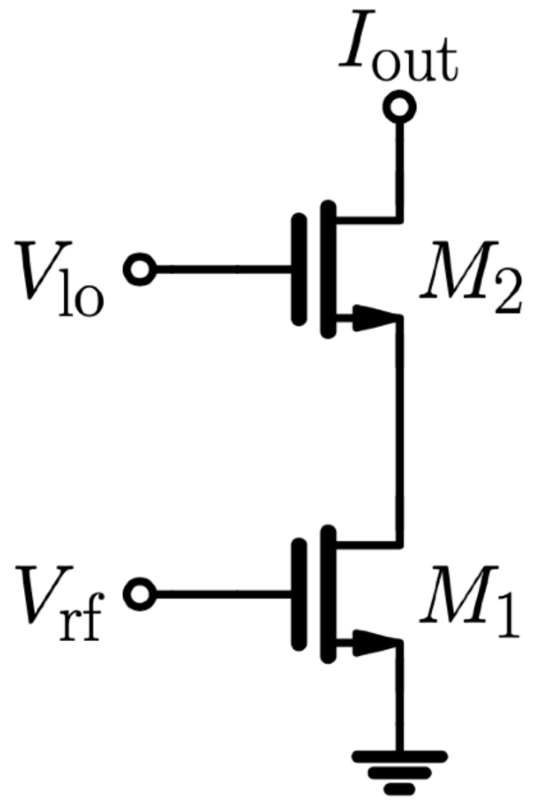


The **cascoded common-source** stage boosts the output impedance of M_1 considerably to $r_{\text{out}} \approx g_{m2}/(g_{ds1} \cdot g_{ds2})$.



[9]

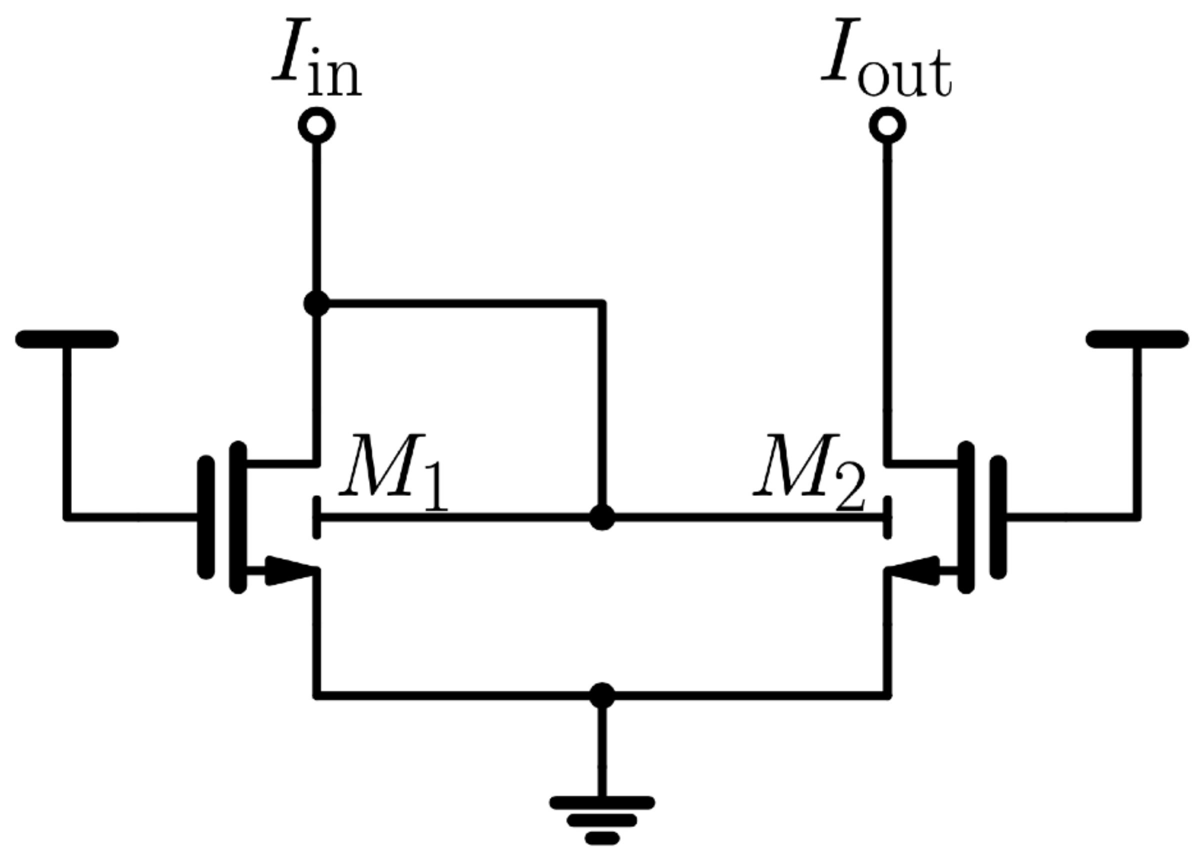
This is a variation of the implementation shown earlier, where the **degeneration** of M_1 can be **adapted** by tuning V_{bias}.



[10]

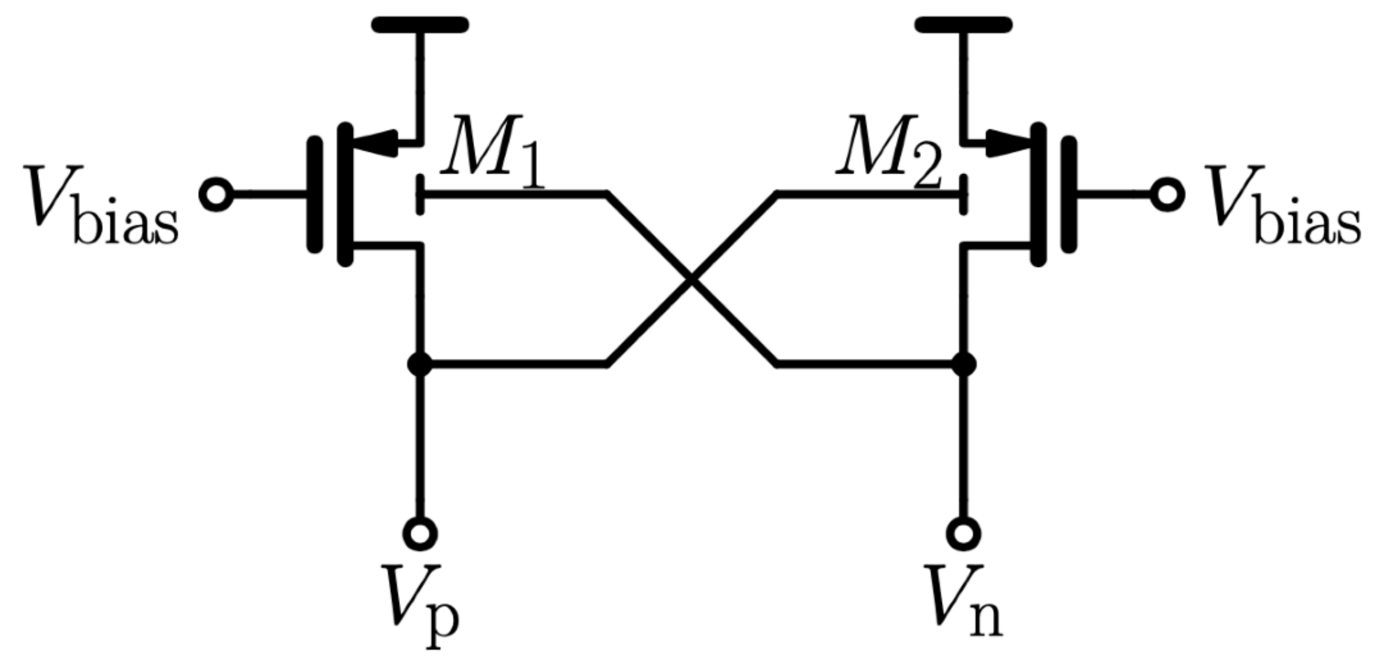
In this **dual-gate MOS-FET mixer**, the periodic local-oscillator signal V_{lo} causes the time-variant change of the transconductance of M_1, resulting in a frequency conversion from the input V_{rf} to the output I_{out}.

Some Use All 4-Terminals of the MOSFET



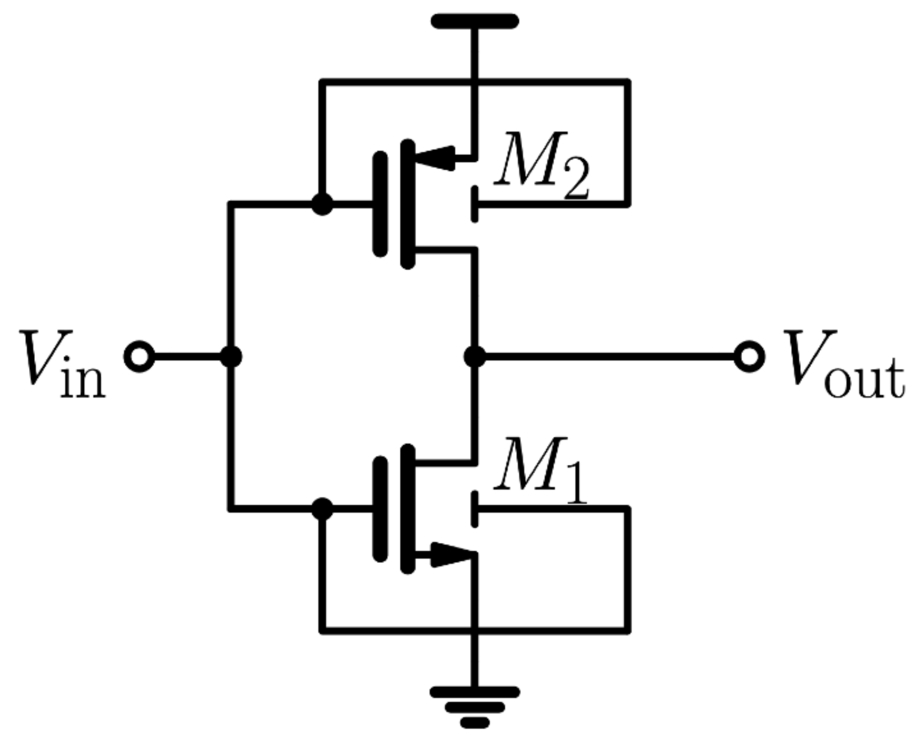
[11]

This circuit is an improved **bulk-driven current mirror** that allows low voltage operation, requiring a voltage headroom substantially less than V_{GS1}.



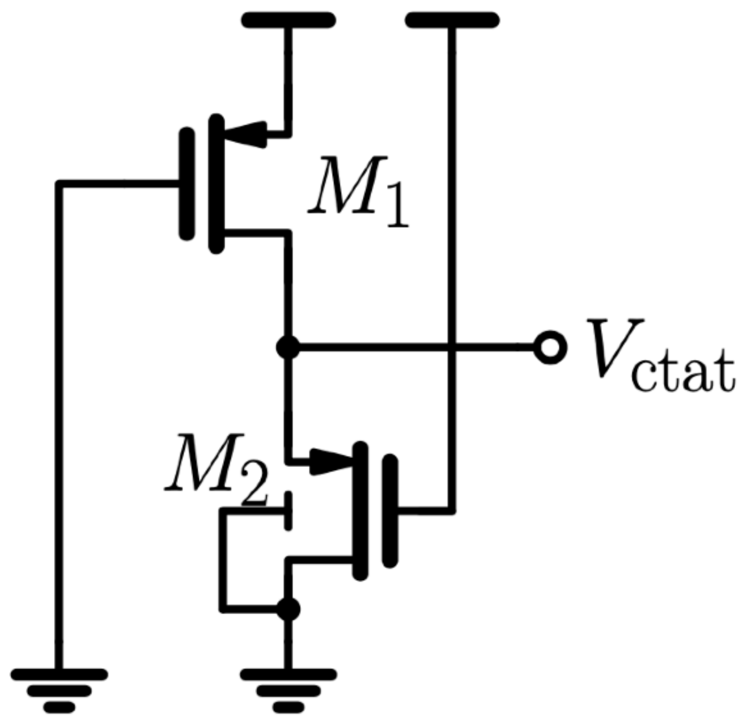
[12]

This circuit is a **low-voltage** version of a **cross-coupled pair**, where the body controls the MOS-FETs, avoiding the significant V_{GS} drop at V_{p} and V_{n}.



[13]

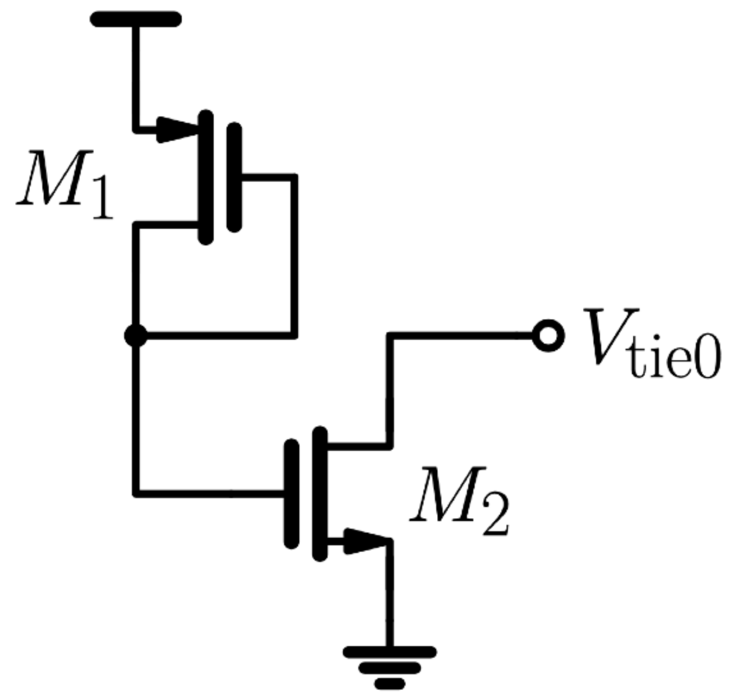
The (dynamic threshold) **DT-MOS inverter** achieves an improved current drive at low leakage current. It needs to be operated at low supply voltages to avoid a forward bias of the well diodes.



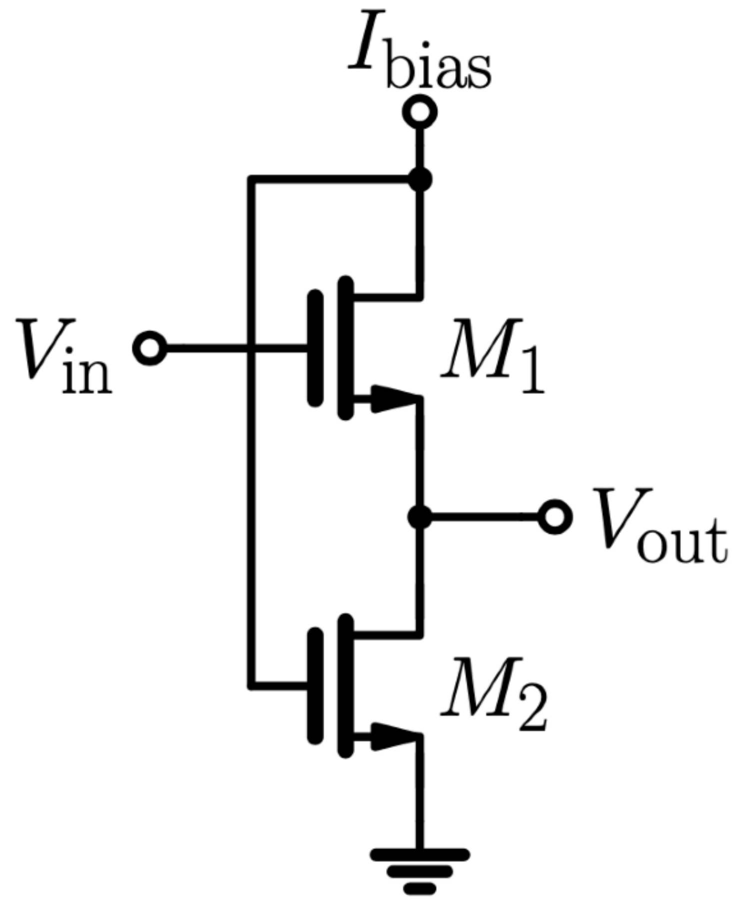
[14]

Exploiting the parasitic (lateral) PNP transistor inherent in a PMOS structure, this simple **CTAT voltage generator** can be created.

Some are Super Useful but Rarely Taught in School

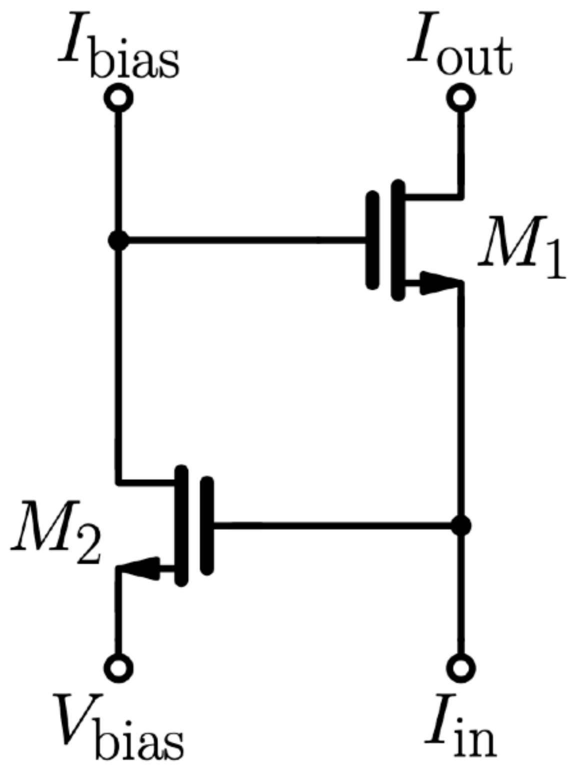


An ESD-safe **tie-zero** for unused CMOS logic inputs (no MOS-FET gate should be tied directly to a supply rail). The tie-one can be constructed accordingly.



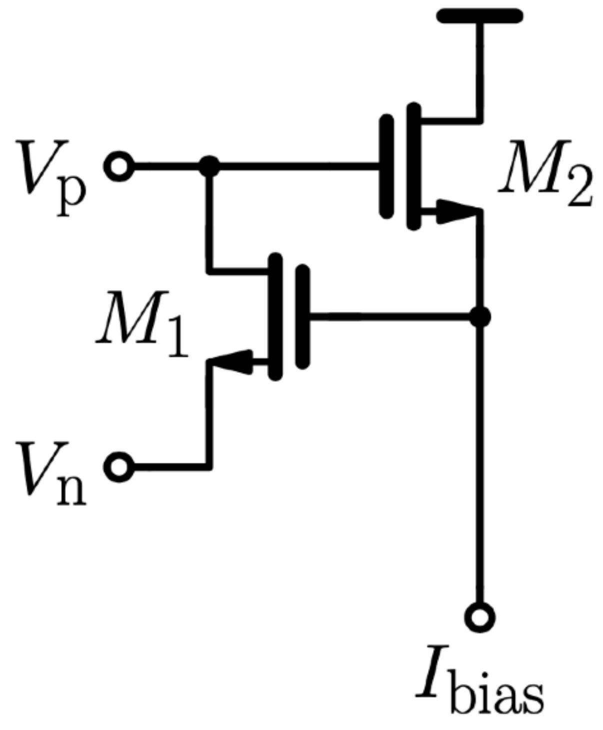
[15]

The **flipped voltage follower** is an improved version of the standard source follower, employing feedback to lower the output impedance to $r_{\text{out}} = g_{ds2}/(g_{m1} \cdot g_{m2})$.



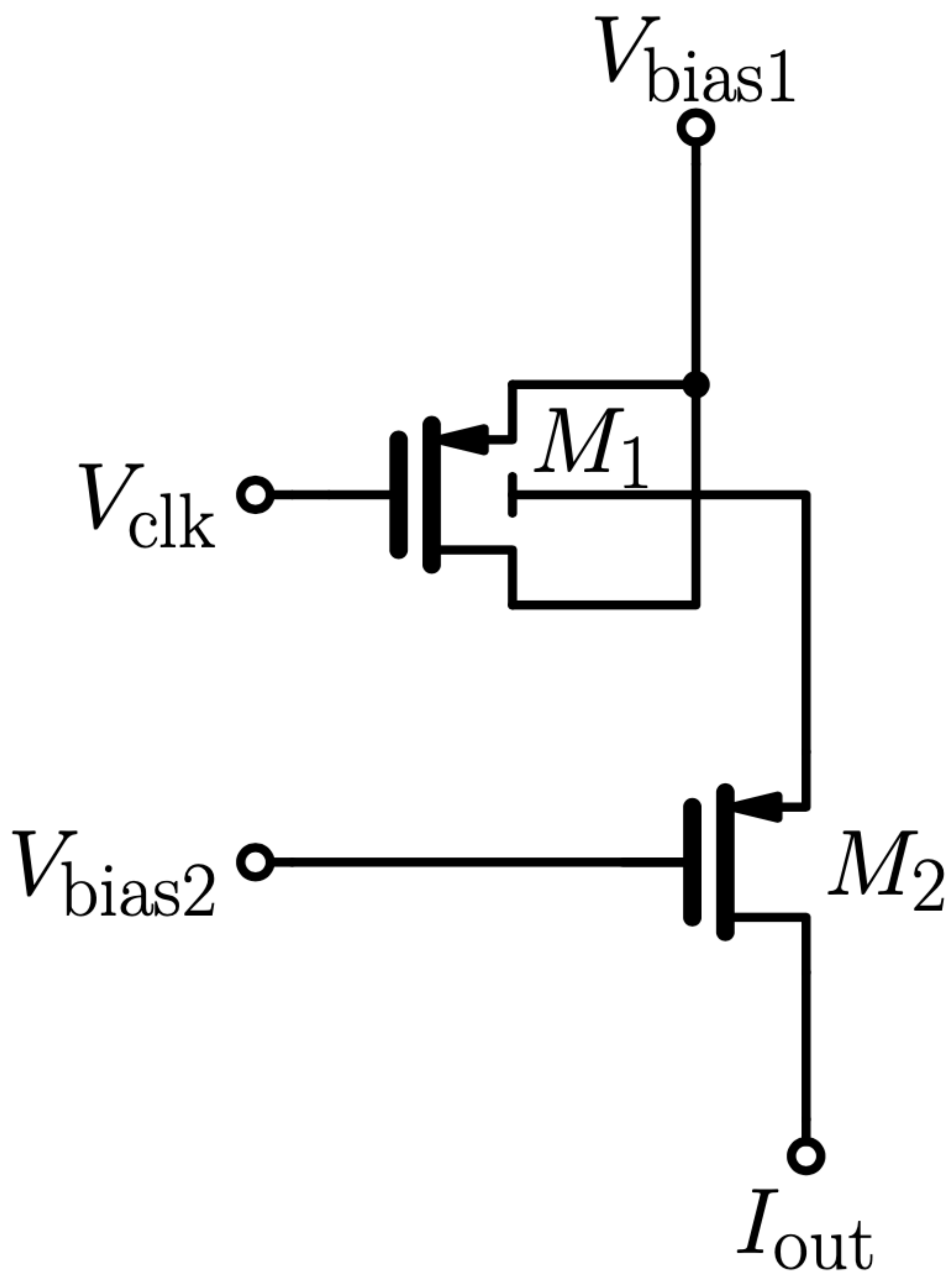
[16]

The **regulated cascode** improves the effect of the cascode M_1 by g_{m2}/g_{ds2} due to feedback. Note that the source of M_2 can be tied to ground if combined with a common-source input stage.



The floating **level shift** (or "floating **battery**") effectively shifts a bias point between V_{p} and V_{n}, as $V_{\text{shift}} = V_{\text{p}} - V_{\text{n}} = V_{\text{GS1}} + V_{\text{GS2}}$.

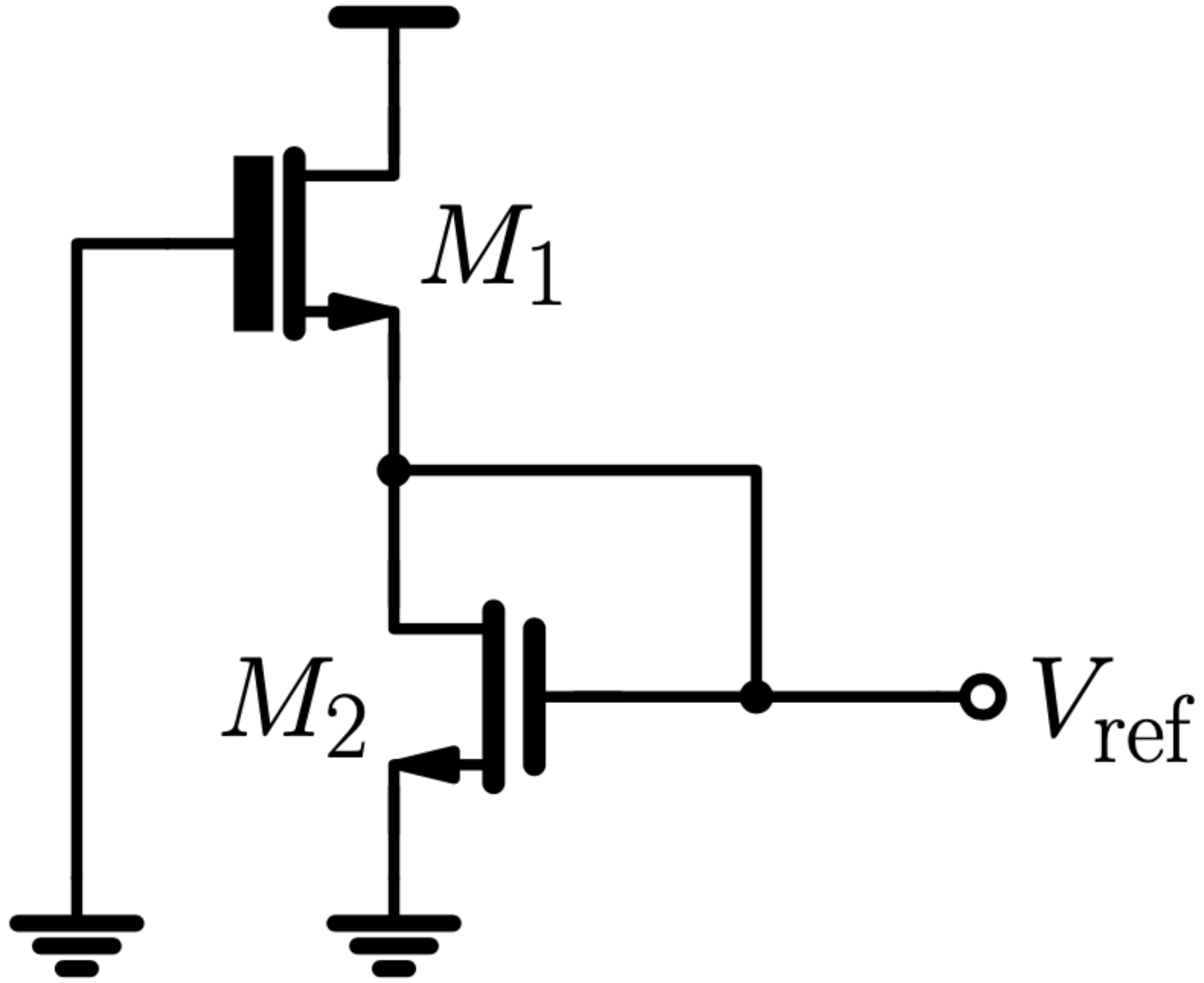
Some are Pretty Clever: pA Current Source



[17]

This **pA current source** is based on the periodic filling and flushing of the Si–SiO_2 interface traps by alternating M_1 between accumulation and inversion. It can operate with reasonably high clock frequencies and still create tiny currents.

Some are Pretty Clever: Voltage Reference

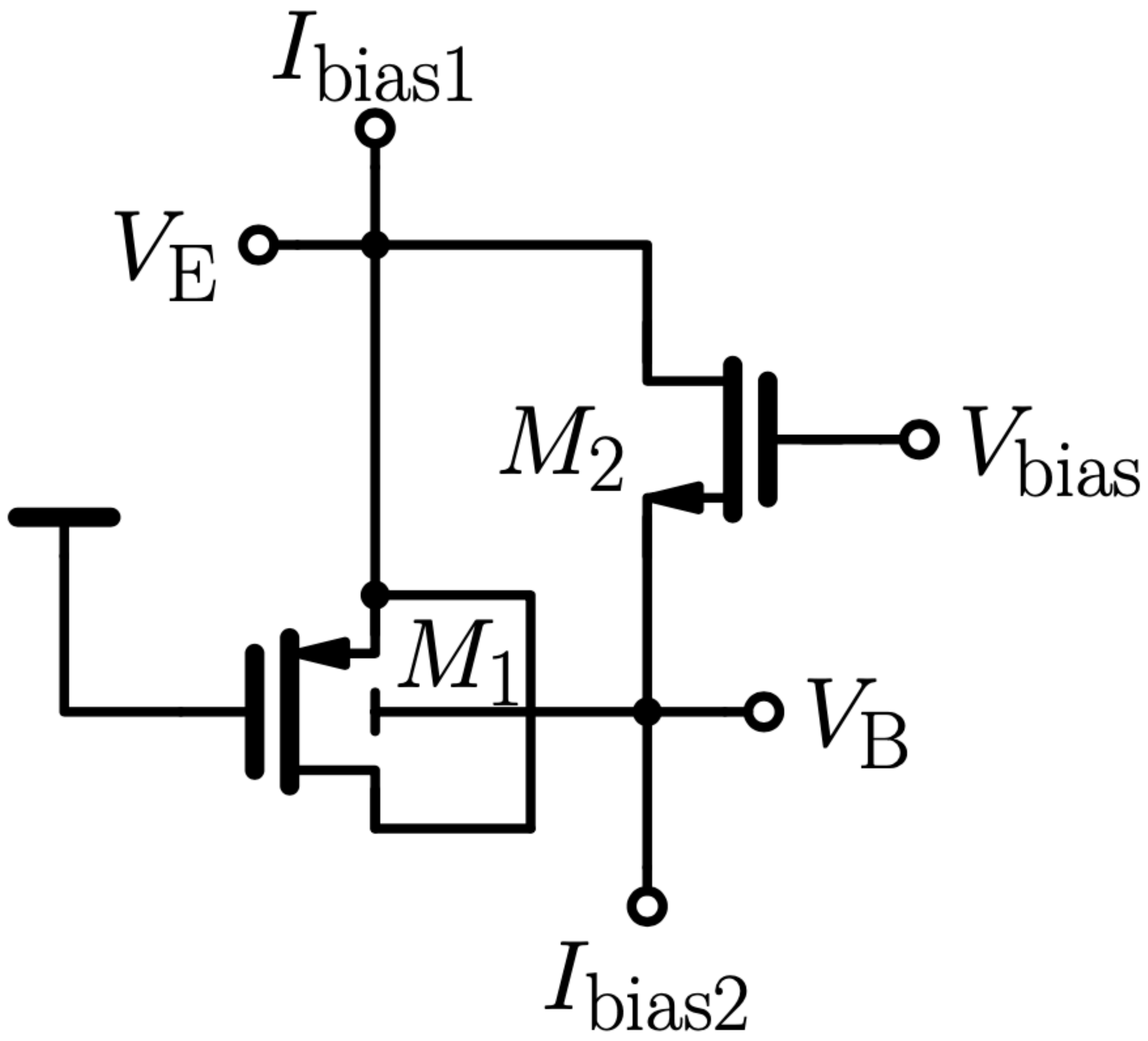


[18]

This **constant bias voltage** generator creates a remarkably stable output voltage (note that M_1 and M_2 must have different threshold voltages $V_{th1} \neq V_{th2}$).

$$V_{ref} = \frac{n_1 n_2}{n_1 + n_2} \left(V_{th2} - V_{th1}\right) + \frac{n_1 n_2}{n_1 + n_2} V_T \ln \left(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1} \right)$$

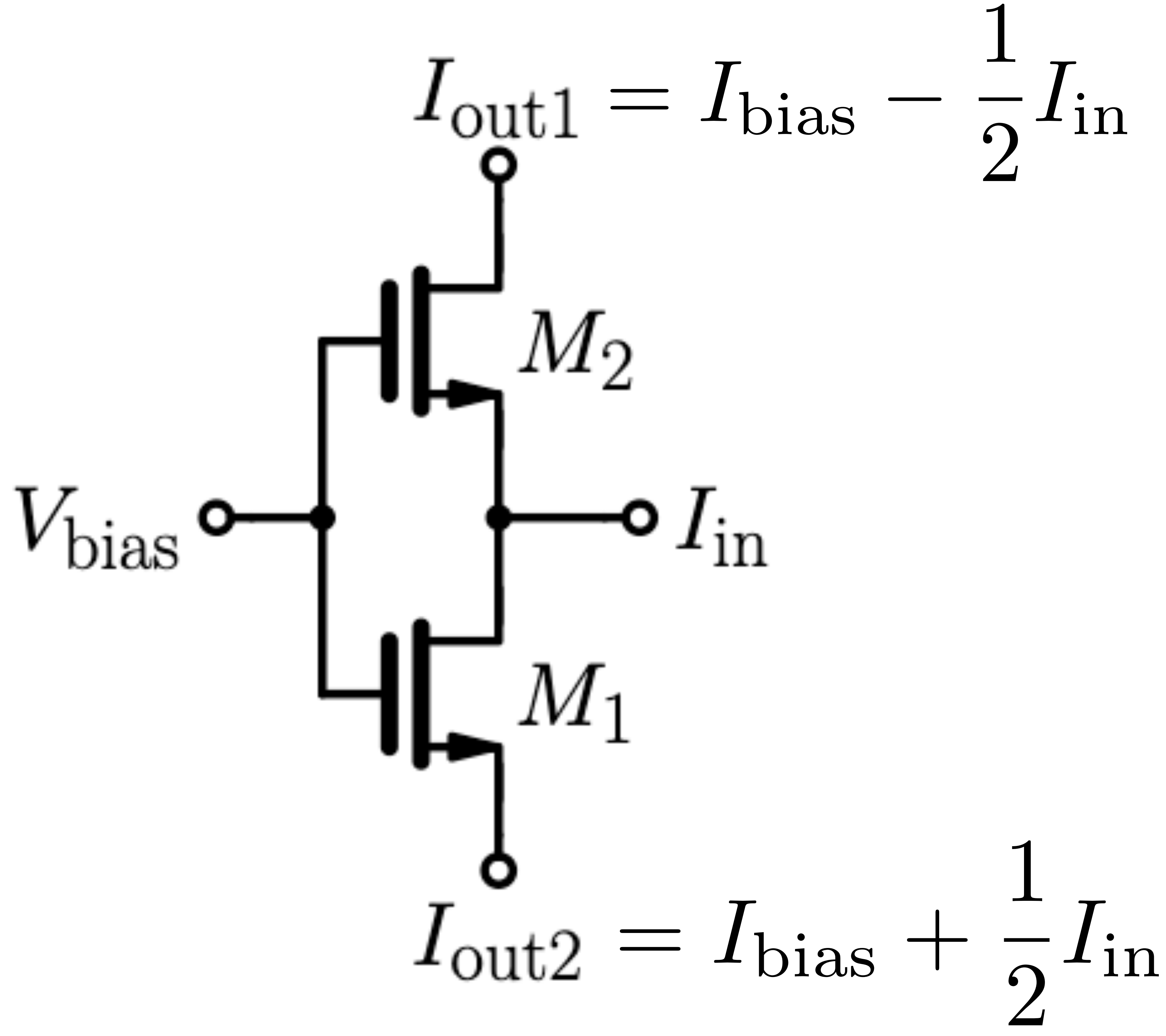
Some are Pretty Clever: PNP I_C Control



[19]

The parasitic BJT (lateral or vertical) often suffers from poor $\beta \ll 10$. This circuit forces the collector current of the parasitic (vertical) **PNP** (realized by M_1) to $I_C = I_{\text{bias1}} - I_{\text{bias2}}$, although the collector terminal (being the p-substrate) is not accessible. By doing this, the resulting $V_{\text{EB}} = V_{\text{E}} - V_{\text{B}}$ can be accurately used in a bandgap circuit.

Some are Pretty Clever: Bult Current Divider



[20]

This implementation is the **Bult current divider** (if M_1 and M_2 are of identical size, then I_{in} is precisely split in half between I_{out1} and I_{out2}).

Final Remarks

- The MOSFET is a wonderful device, despite all its quirks — try a hand calculation of g_m or g_{ds} in a nm-device.
- One would think that all useful two-transistor circuits have long been invented — this does not seem to be the case.
- You never know how MOSFETs are used in a circuit — thus need models that work well in all kinds of operating modes and bias conditions.

References

[1] H. Pretl and M. Eberlein, "Fifty Nifty Variations of Two-Transistor Circuits: A tribute to the versatility of MOSFETs," in IEEE Solid-State Circuits Magazine, vol. 13, no. 3, pp. 38-46, Summer 2021, DOI:10.1109/MSSC.2021.3088968.
[2] E. A. M. Klumperink, F. Bruccoleri, and B. Nauta, “Finding all elementary circuits exploiting transconductance,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 48, no. 11, pp. 1039–1053, 2001. DOI:10.1109/82.982356.
[3] D. Shahhosseini, E. Zailer, L. Behjat, and L. Belostotski, “Method of generating unique elementary circuit topologies,” *Can. J. Elect. Comput. Eng.*, vol. 41, no. 3, pp. 118–132, 2018. DOI:10.1109/CJECE .2018.2859621.
[4] F. Wanlass and C. Sah, “Nanowatt logic using field-effect metal-oxide semiconductor triodes,” in Proc. IEEE ISSCC Dig. Tech. Papers, 1963, pp. 32–33. DOI:10.1109/ISSCC.1963.1157450.
[5] R. Widlar, “Some circuit design techniques for linear integrated circuits,” IEEE Trans. Circuit Theory, vol. 12, no. 4, pp. 586–590, 1965. DOI:10.1109/TCT.1965.1082512.
[6] A. D. Blumlein, “Thermionic valve amplifying circuit,” U.S. Patent 2 185 367, 1937.
[7] F. Krummenacher, E. Vittoz, and M. Degrauwe, „Class AB CMOS amplifier micropower SC filters,“ Electron. Lett., vol. 17, no. 13, pp. 433-435, 1981. DOI:10.1049/el:19810304.
[8] B. Nauta and E. Seevinck, “Linear CMOS transconductance element for VHF filters,” Electron. Lett., vol. 25, no. 7, pp. 448–450, Mar. 1989. DOI:10.1049/el:19890308.
[9] W. Sansen, Analog Design Essentials. New York: Springer-Verlag, 2006. DOI:10.1109/ISCAS.1995.523807.
[10] S. C. Cripps, O. Nielsen, D. Parker, and J. A. Turner, “An experimental evaluation of X-band mixers using dual-gate GaAs MESFETs,” in Proc. 1977 7th Eur. Microw. Conf., pp. 101–104. DOI:10.1109/ EUMA.1977.332410.
[11] B. J. Blalock and P. E. Allen, “A low-voltage, bulk-driven MOSFET current mirror for CMOS technology,” in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), 1995, pp. 1972–1975.
[12] S. Chatterjee, Y. Tsividis, and P. Kinget, “0.5-V analog circuit techniques and their application in OTA and filter design,” IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2373–2387, 2005. DOI:10.1109/JSSC.2005.856280.
[13] F. Assaderaghi, S. Parke, D. Sinitsky, J. Bokor, P. K. Ko, and C. Hu, “A dynamic threshold voltage MOSFET (DTMOS) for very low voltage operation,” IEEE Electron Device Lett., vol. 15, no. 12, pp. 510–512, 1994. DOI:10.1109/55.338420.
[14] E. A. Vittoz, “MOS transistors operated in the lateral bipolar mode and their application in CMOS technology,” IEEE J. Solid-State Circuits, vol. 18, no. 3, pp. 273–279, 1983. DOI:10.1109/JSSC.1983.1051939.
[15] J. Ramirez-Angulo, R. G. Carvajal, A. Torralba, J. Galan, A. P. Vega-Leal, and J. Tombs, “The flipped voltage follower: A useful cell for low-voltage low-power circuit design,” in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), 2002, p. III. DOI:10.1109/ISCAS.2002.1010299.
[16] B. J. Hosticka, “Improvement of the gain of MOS amplifiers,” IEEE J. Solid-State Circuits, vol. 14, no. 6, pp. 1111–1114, 1979. DOI:10.1109/JSSC.1979.1051324.
[17] U. Cilingiroglu, A. Becker-Gomez, and K. T. Veeder, “An evaluation of MOS interface-trap charge pump as an ultralow constant-current generator,” IEEE J. Solid-State Circuits, vol. 38, no. 1, pp. 71–83, 2003. DOI:10.1109/JSSC.2002.806282.
[18] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, “A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 V,” IEEE J. Solid-State Circuits, vol. 47, no. 10, pp. 2534–2545, 2012. DOI:10.1109/JSSC.2012.2206683.
[19] M. Eberlein, “Bandgap reference circuit with beta-compensation,” U.S. Patent 9 568 929 B2, Feb. 14, 2017.
[20] K. Bult and G. J. G. M. Geelen, “An inherently linear and compact MOST-only current division technique,” *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1730–1735, 1992. DOI:10.1109/4.173099.

Thank You!