GigaDevice Semiconductor Inc.

Device limitations of GD32F45x/F40x

Errata Sheet

Table of Contents

List of Figures

List of Tables

1. Introduction

This document applies to GD32F45x/F40x product series, as shown in ***Table 1-1. Applicable products***. It provides the technical details that need to be paid attention to in the process of using GD32 MCU, as well as solutions to related problems.

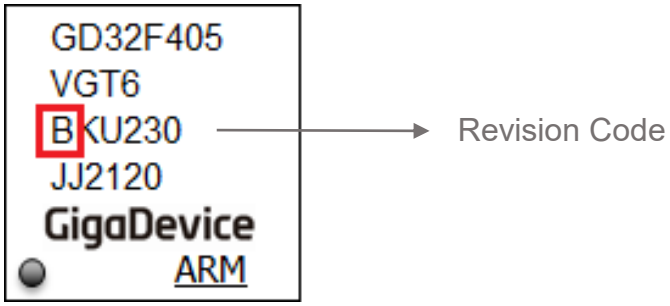
Table 1-1. Applicable products

Type	Part Numbers
MCU	GD32F405xx series
	GD32F407xx series
	GD32F450xx series

1.1. Revision identification

The device revision can be determined by the mark on the top of the package. The 1st code on the line 3 of the mark represents product revision code. As the picture shown in ***Figure 1-1. Device revision code of GD32F45x/F40x***.

Figure 1-1. Device revision code of GD32F45x/F40x



1.2. Summary of device limitations

The device limitations of GD32F45x/F40x are shown in ***Table 1-2. Device limitations***, please refer to section 2 for more details.

Table 1-2. Device limitations

Module	Limitations	Workaround
		Rev. Code B
RCU	*System operation fails due to system clock switching from high clock frequency to low clock frequency*	Y
GPIO	*Pin voltage level difference between PA11 and PA12 influences the power*	Y
DMA	*DMA channel counter reconfigures*	Y
	DMA burst transmission faults	N

Module	Limitations	Workaround
		Rev. Code B
IPA	*One extra pixel will be transferred*	N
ADC	*ADC samples abnormally when using both 6-bit sampling resolution and MSB alignment*	Y
	ADC alignment mode is not consistent with the user manual description	Y
RTC	*Calibrate abnormally when using both smooth digital calibration and FREQI calibration*	Y
TIMER	*The shadow preloaded value takes effect only on the rising edge of the counter after modification*	N
	Count error when timer works at single pulse mode	Y
USART	*Mute mode can be waked up as long as the USART_CTL0 register is operated after mute mode is enabled*	Y
I2C	*I2C_FCTL register is only configurable on GD32F450xx*	N
EXMC	*SDRAM controller can not be used time-shared with other EXMC controller*	N
	DSET bits and ASET bits configurations are invalid when NDWTEN bit is set	N
ENET	*Data reception faults in MII mode*	Y
	Reception data frame is dropped when enable hardware checksum and the header checksum is 0x0000	Y

Note:

Y = Available;

N = Not available.

2. Descriptions of device limitations

2.1. RCU

2.1.1. System operation fails due to system clock switching from high clock frequency to low clock frequency

Description & impact

System operation fails when system clock switching from high clock frequency (more than 120MHz) to low clock frequency.

Workarounds

Firstly, reduce the system frequency (such as HCLK / 2 or HCLK / 4); secondly, delay more than 20 HCLK clock; finally, switch to the low clock frequency.

2.2. GPIO

2.2.1. Pin voltage level difference between PA11 and PA12 influences the power consumption in deep-sleep mode

Description & impact

Pin level difference between PA11 and PA12 influences the power consumption in deep-sleep mode.

Workarounds

Keep the same pin level on PA11 and PA12.

2.3. DMA

2.3.1. DMA channel counter reconfigures unsuccessfully

Description & impact

DMA channel counter reconfigures unsuccessfully.

Workarounds

Clear full transfer finish flag (FTFIFx) and half transfer finish flag (HTFIFx) before reconfiguring the DMA channel counter.

2.3.2. DMA burst transmission faults

Description & impact

The rest of data bytes that is less than fifo depth generates transmission error when using DMA burst transmission.

Workarounds

Not available.

2.4. IPA

2.4.1. One extra pixel will be transferred

Description & impact

One extra pixel will be transferred when using register value to memory direction.

Workarounds

Not available.

2.5. ADC

2.5.1. ADC samples abnormally when using both 6-bit sampling resolution and MSB alignment

Description & impact

ADC samples abnormally when using both 6-bit sampling resolution and MSB alignment mode.

Workarounds

Use LSB alignment mode or use 8-bit sampling resolution.

2.5.2. ADC alignment mode is not consistent with the user manual description

Description & impact

ADC alignment mode is not consistent with the user manual description.

Workarounds

The right alignment mode description is as follow:

Table 2-1. Alignment mode of routine conversion

Alignment	Resolution	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
LSB	12bit	0x0				data											
	10bit	0x0				data										0x0	
	8bit	0x0				data									0x0		
	6bit	0x0				data								0x0			
MSB	12bit	data												0x0			
	10bit	data											0x0				
	8bit	data										0x0					
	6bit	invalid															

2.6. RTC

2.6.1. Calibrate abnormally when using both smooth digital calibration and FREQI calibration

Description & impact

Using both smooth digital calibration and FREQI calibration will cause calibration result abnormal.

Workarounds

1) Use RTC shift function to replace smooth digital calibration, such as setting A1S bit and configuring appropriate SFS bits to satisfy the accuracy requirement.
2) Use two 16 seconds calibration window to replace one 32 seconds calibration window.

2.7. TIMER

2.7.1. The shadow preloaded value takes effect only on the rising edge of the counter after modification

Description & impact

The preloaded value takes effect only on the rising edge of the counter after modification which may cause problem to pwm applications with high timing requirements.

Workarounds

Not available.

2.7.2. Count error when timer works at single pulse mode

Description & impact

Timer works at single pulse mode and CK_APBx is CK_AHB / 4 and CK_TIMER is CK_AHB / 2, which causes count error.

Workarounds

1) Do not use above clock configuration.
2) Use timer update interrupt to clear error count.

2.8. USART

2.8.1. Mute mode can be waked up as long as the USART_CTL0 register is operated after mute mode is enabled

Description & impact

After mute mode is enabled, the operation on USART_CTL0 register will wake up USART from mute mode.

Workarounds

When mute mode is enabled and USART uses hardware method to detect idle frame wakeup, operation on USART_CTL0 register is not allowed. When mute mode is enabled and USART uses software method to detect idle frame wakeup, operation on USART_CTL0 register only be allowed when need to exit mute mode.

2.9. I2C

2.9.1. I2C_FCTL register is only configurable on GD32F450xx

Description & impact

The filter control register (I2C_FCTL) is only configurable on GD32F450xx but not on GD32F405xx or GD32F407xx.

Workarounds

Not available.

2.10. EXMC

2.10.1. SDRAM controller can not be used time-shared with other EXMC controller

Description & impact

SDRAM controller can not be used time-shared with other EXMC controller.

Workarounds

Not available.

2.10.2. DSET bits and ASET bits configurations are invalid when NDWTEN bit is set

Description & impact

Data setup time (DSET) and address setup time (ASET) configurations are invalid when wait function is enabled.

Workarounds

Not available.

2.11. ENET

2.11.1. Data reception faults in MII mode

Description & impact

ENET_MII_COL / ENET_MII_CRS / ENET_MII_RX_ER pins are floating on MCU and external PHY has no these pins,.which will cause data reception faults.

Workarounds

Configure ENET_MII_COL pin and ENET_MII_RX_ER pin as AF function and keep them low level. The ENET_MII_CRS pin mode and status can be ignored.

2.11.2. Reception data frame is dropped when enable hardware checksum and the header checksum is 0x0000

Description & impact

When enable hardware checksum and header checksum is 0x0000, this frame will be mistaken for error frame and dropped by hardware.

Workarounds

Use software checksum.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jun.20 2022

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